Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

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**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: C = .004” X .005” B/E = .003” X .003”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .027” X .030” DATE: 7/21/22**

**MFG: LINEAR SYSTEMS THICKNESS .008” P/N: LS318**

**DG 10.1.2**

#### Rev B, 7/19/02